IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application		)	PATENT APPLICATION
Inventor(s):	Frederick Ware, et al.	)	
		)	Art Unit: 2829
Application No.:	10/768,443	)	
		)	Examiner: Nguyen, T.
Filed:	January 30, 2004	)	
Title:	METHOD AND APPARATUS FOR TEST CHARACTERIZATION OF SEMICONDUCTOR COMPONENTS	)	**Customer No. 38456**

DECLARATION OF SCOTT C. BEST PURSUANT TO 37 C.F.R. §1.131

I, SCOTT C. BEST, declare that:

1. I am a co-inventor of the invention described and claimed in the above-identified patent application. I am currently a Senior Principal Design Engineer employed by Rambus Inc. (Rambus), assignee of the above-identified patent application. The above-identified application claims priority to U.S. Provisional Application No. 60/450,007, entitled "METHOD AND APPARATUS FOR TEST AND CHARACTERZATION OF SEMICONDUCTOR COMPONENTS", filed February 23, 2003. I have reviewed the pending application as stated in my Declaration for Patent Application and the pending claims as set forth in the RESPONSE TO OFFICE ACTION ("RESPONSE") accompanying this DECLARATION. I have also reviewed U.S. Publication No. 2008/0049819 A1 ("*Garlett, et al.* reference") having an application filing date of July 9, 2002 ("Effective Date") which has been cited against the above-identified patent application.

2. I understand that this DECLARATION will be filed in the United States Patent and Trademark Office in order to provide factual evidence showing that the subject matter claimed in the above-identified patent application was conceived prior to the Effective Date and with due diligence was constructively reduced to practice by filing the above-identified patent application.

3. The facts set forth hereinafter to establish that the subject matter of the above-identified patent application was conceived and reduced to practice prior to the Effective Date relate to acts which occurred and were carried out within the United States of America.

4. I received a Bachelor of Science in Electrical Engineering (B.S.E.E.) degree from Cornell University in New York, 1989.

5. I have extensive design experience in mixed-signal circuits and systems at Rambus, VLSI Technology, Cypress Semiconductor and National Semiconductor from 1989 to the present.

6. Rambus is based in Los Altos, California and was incorporated in 1990. Rambus specializes in the invention and design of high-speed chip interfaces that are included in a wide range of consumer, computing and communications applications.

7. I am currently a Senior Principal Design Engineer at Rambus responsible for clock-generation and timing circuits in a micro-processor interface. I have also contributed to the design of interfaces in a variety of integrated circuit memory devices.

8. I am at least a co-inventor of over 25 filed United States of America utility patent applications.

9. I am at least a co-inventor of at least 13 issued Unites States of America utility patents.

10. I, along with my co-inventors, conceived of the subject matter of the present claims in the above-identified patent application prior to the Effective Date of the *Garlett, et al.* reference.

11. I, along with my co-inventors, acted with due diligence from at least a conception date of April 3, 2002, to the filing of the above-identified patent application. While I am providing factual evidence by way of the accompanying Exhibits and this DECLARATION of at least a conception

date of April 3, 2002, additional evidence supports an earlier conception date and further due diligence. Accordingly, this DECLARATION and the accompanying Exhibits should not be construed in any way to limit the subject matter of the above-identified patent application to a conception date of April 3, 2002.

12. In 2002, co-inventor Timothy Chang held weekly "test meetings" to foster built-in self-test ("BIST") ideas.

13. Exhibit A is a copy of a page of my notes that I wrote in 2002. The passage under "3Apr02" was contemporaneously written during a test meeting ("YS test meeting") on April 3, 2002. Among other entries, I wrote: "A-byte IO tied to B-byte IO. skew one to affect the other". This entry refers to using one byte at the I/O interface to test another byte during BIST.

14. Exhibit B is a copy of an email dated June 26, 2002 from Rob Dhat, a Rambus employee, to other Rambus employees attaching schematics and describing the progress of the TC2 ("Test Chip 2") Marketing Board and TC3 ("Test Chip 3") Test Board. The TC2 Marketing Board and TC3 Test Board include embodiments of the claimed invention.

15. Exhibit C is an email dated July 10, 2002 from a Rambus employee, Philip Yeung, to co-inventor Ely Tsern, requesting a customer demonstration date for the TC3 Test Board and identifying items to be completed.

16. Exhibit D is a copy of an email dated July 12, 2002 from Rob Dhat to Rambus employees attaching the TC3 Test Board schematics for review.

17. Exhibit E is a copy of the TC3 Test Board schematics that was attached to the e-mailed dated July 12, 2002.

18. Exhibit F is a copy of an email dated July 26, 2002 from Philip Yeung to Rambus employees describing package and board releases for the TC3 Test Board.

19. Exhibit G is a copy of a "Rambus Invention Disclosure Form" identified as "RD-266" dated July 18, 2008 describing embodiments of the claimed invention which was provided by co-inventor Frederick A. Ware.

20. Exhibit H is a copy of an e-mail dated October 2, 2002 from the patent attorney who drafted the provisional application, Barbara Courtney, attaching a draft application for the inventors' review.

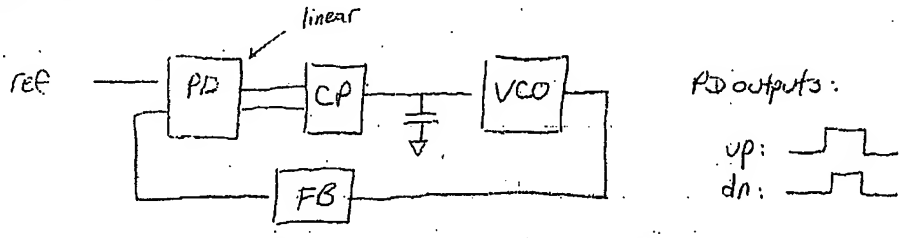
21. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 1 Dec 08

By: _____
Scott S. Best
Senior Principal Design Engineer
Rambus Inc.

29 Mar 02

- Tim's YAC test meeting
  - ↳ PLL self-check idea



  - ↳ want to put a latch into the CP: if up leads dn, latch 1, else latch 0.
    - ⇒ check this latch's output for 64 samples
    - ⇒ problem: comparator has offset which will dominate PD outputs ⇒ look after CP
  - ↳ put 3 ISamps per pair, use "Vref" to test Vcm of each output during test mode

1 Apr 02

- testchip 3 meeting
  - ↳ present numbers for SSTL drivers. Like what?
    - ⇒ duty cycle, ISI jitter
    - ⇒ something to sim in SSTL; Catherine seeing bad waveforms?

3 Apr 02

- Ref-YAC work
  - ↳ inheriting all PLL stuff from Ying
  - ↳ inheriting all current-cal and Rcal from Ying
  - ↳ all dual-mode IO pieces going to Anthony

- XS test meeting
  - ↳ skew Iref (glxa, Iout) per byte with a scan chain
    - ⇒ A-byte IO tied to B-byte IO, skew one to affect the other
    - ⇒ worst case is 50mV swing off Vdd (Vcm = Vdd - 25mV)
  - ↳ set Iref bits with a scan chain at each byte
    - ⇒ Rx and Tx mode need to be affected together

4 Apr 02

- Redpoint on tester:
  - → can see DQS's being generated during a WRITE (voltage-mode)
    - ⇒ ugly waveforms edges. Board term or source noise?
  - → want to see: DQ & related to DQS at mem device
    - ⇒ where to trigger??? DQ should be clean...

0804CL

EXHIBIT A

Wendy Goy

From: Dhat, Rob [rdhat@rambus.com]
Sent: Wednesday, June 26, 2002 12:13 PM
To: Yeung, Philip
Cc: Echevarria, Victor; Dhat, Rob
Subject: TC2.1 respin board and unofficial TC3 test board schematics

Attachments: @

@ (206 B)

This message has been archived. View the original item
http://entvaultdir/EnterpriseVault/ViewMessage.asp?VaultId=
1AAE4F7E27DA3F74BA32885FF7A69B5891110000entvaultdir&SavesetId=536000000000000~
200206261912410000~1~E7102B6F58C14EEEAA9BA68E0462F6B

I've attached 2 sets of schematics:

1. TC2 Marketing Board - essentially what was sent to RDF yesterday minus a few bugs that were discovered over the weekend.

2. TC3 Test Board - core of what will exist on the board is there however there is an ongoing debate as to what else we should/shouldn't implement.I'm calling a meeting this afternoon we can iron out this debate.Will add you guys to the list.

--
Rob Dhat
Email rdhat@rambus.com
Direct 650.947.5364
Fax 650.947.5001
--

Attachments:
tc3_tst_r01.pdf (1.8 MB)
http://entvaultdir/EnterpriseVault/ViewMessage.asp?VaultId=
1AAE4F7E27DA3F74BA32885FF7A69B5891110000entvaultdir&SavesetId=536000000000000~
200206261912410000~1~E7102B6F58C14EEEAA9BA68E0462F6B&AttachmentId=1

ytrac_demo_marketing_tc2.pdf (1.8 MB)
http://entvaultdir/EnterpriseVault/ViewMessage.asp?VaultId=
1AAE4F7E27DA3F74BA32885FF7A69B5891110000entvaultdir&SavesetId=536000000000000~
200206261912410000~1~E7102B6F58C14EEEAA9BA68E0462F6B&AttachmentId=2

EXHIBIT B

Wendy Goy

From: Yeung, Philip [pyeung@rambus.com]
Sent: Wednesday, July 10, 2002 10:20 PM
To: Tsern, Ely
Cc: Dhat, Rob; Abhyankar, Abhijit; Yuan, Chuck; Kaskey, Jeff; Secker, Dave
Subject: testboard 3 status

Hello Ely,

Could you help to get the date for testchip3 customer demo? In the SPD meeting, I heard we might have a customer demo in early Sept.

We are assuming testchip 3 will use testchip2 package and board to do the initial bringup.

Here are the dependencies we need to resolve before we can release testboard 3. The bottom line is that we might be able to release the board & package by next week. We most likely will be able to get the board and package back by the end of this month.

1. Dave R PCB time
Currently, he is very busy trying to deal with all the Intel related activities.
We probably need 1 -2 days of his time to finish up the design. The design has been sitting for couple of days.

AR: PY will talk to Dave tomorrow trying to get an estimate on his time availability.
We might have to escalate this issue.

2. Final package pinout checking & release
AR: Dave R will call the package house to have them work on the final changes and get obtain the final netlist for checking.

3. Final "system level design review"
AR: Rob will schedule the "final" system design review this week

4. Debug testboard 2

AR: Rob will send out testboard 2.1 (the one on Abhijit's desk) tomorrow morning to load the chips. By friday, we should be in a position to start replicating the bug. Once we can replicate the issue, Wemdem and Victor will continue the debugging.

AR: We'll have a meeting tomorrow morning to discuss debugging strategies

thanks

-- Philip

EXHIBIT C

Wendy Goy

From: Dhat, Rob [rdhat@rambus.com]
Sent: Friday, July 12, 2002 5:50 PM
To: Abhyankar, Abhijit; Chen, Catherine; Wong, Anthony; Best, Scott
Cc: Yeung, Philip; Dhat, Rob
Subject: TC3 Testboard Schematics

Attachments: tc3_tst_r01.pdf

tc3_tst_r01.pdf
(2 MB)

Hello:

I've attached the most recent TC3 testboard schematics. Please review them as soon as you have a chance. I will schedule a final schematic review/signoff meeting monday afternoon to go over any issues discovered. The goal is to tape out the board as soon as possible. Thanks for you help!

--
Rob Dhat
Email rdhat@rambus.com
Direct 650.947.5364
Fax 650.947.5001
--

EXHIBIT D

PAGE 1 LEFT INTENTIONALLY BLANK

RESERVED FOR TABLE CONTENTS

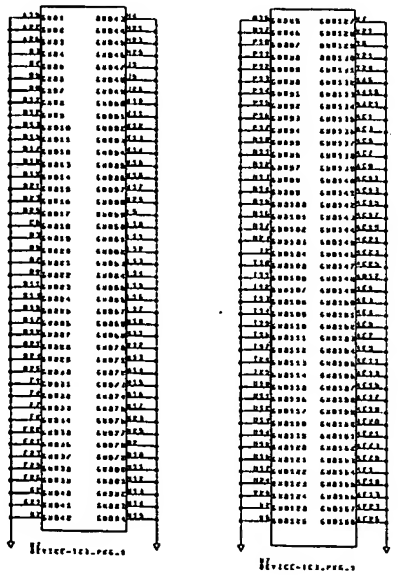
EXHIBIT E

Master/Slave

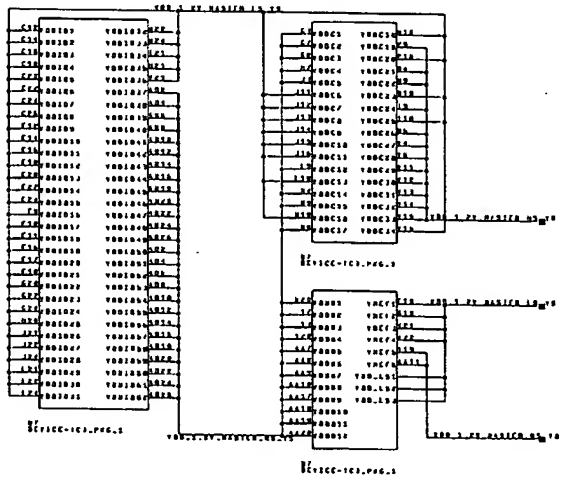
Yellowstone Configuration

MASTER

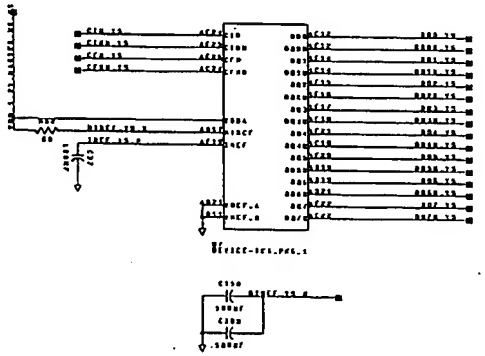
TC3 Package GND Pins



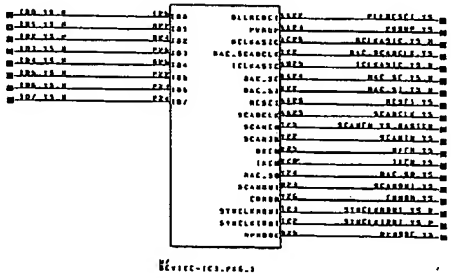
TC3 Package VDD Pins



TC3 Package HS Pins

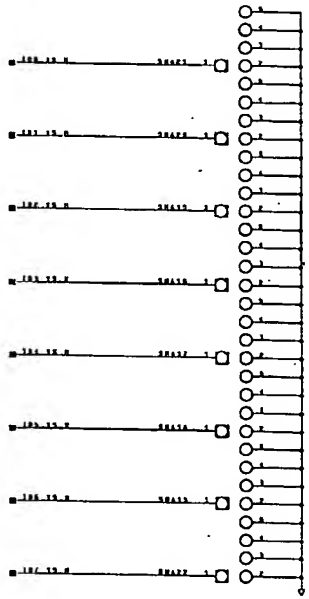


TC3 Package LS Pins



master device specific

TD[0:7] connections

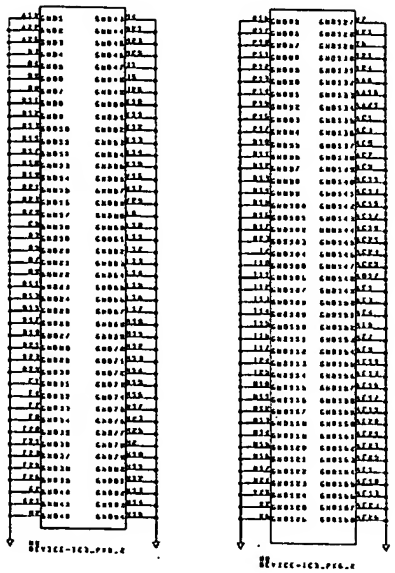


Mester/Slave

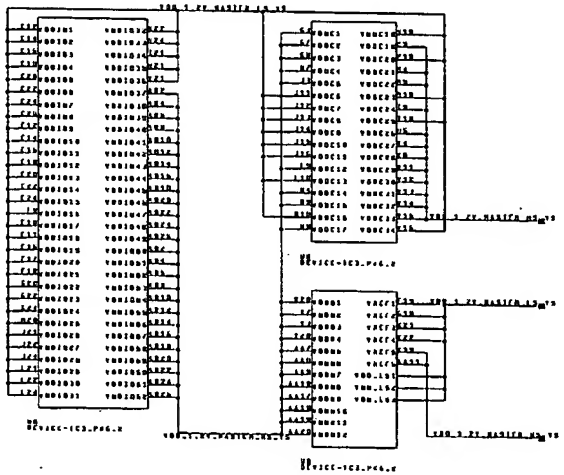
Yellowstone Configuration

SLAVE

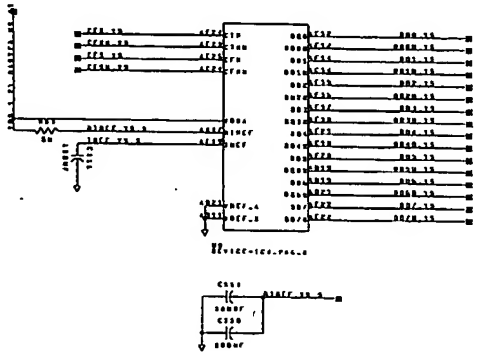
TC3 Package GND Pins



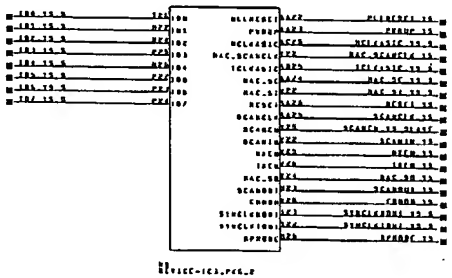
TC3 Package VDD Pins



TC3 Package HS Pins

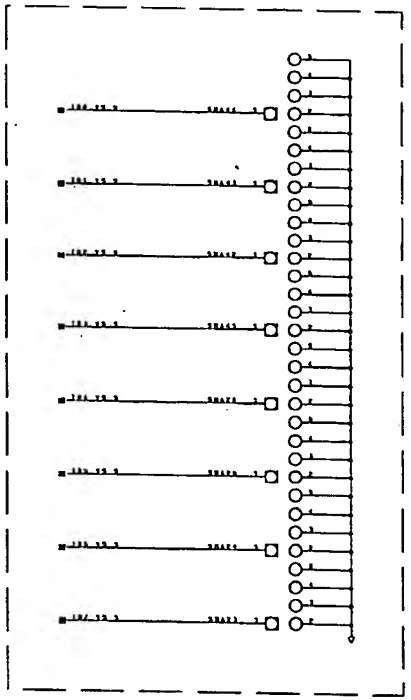


TC3 Package LS Pins

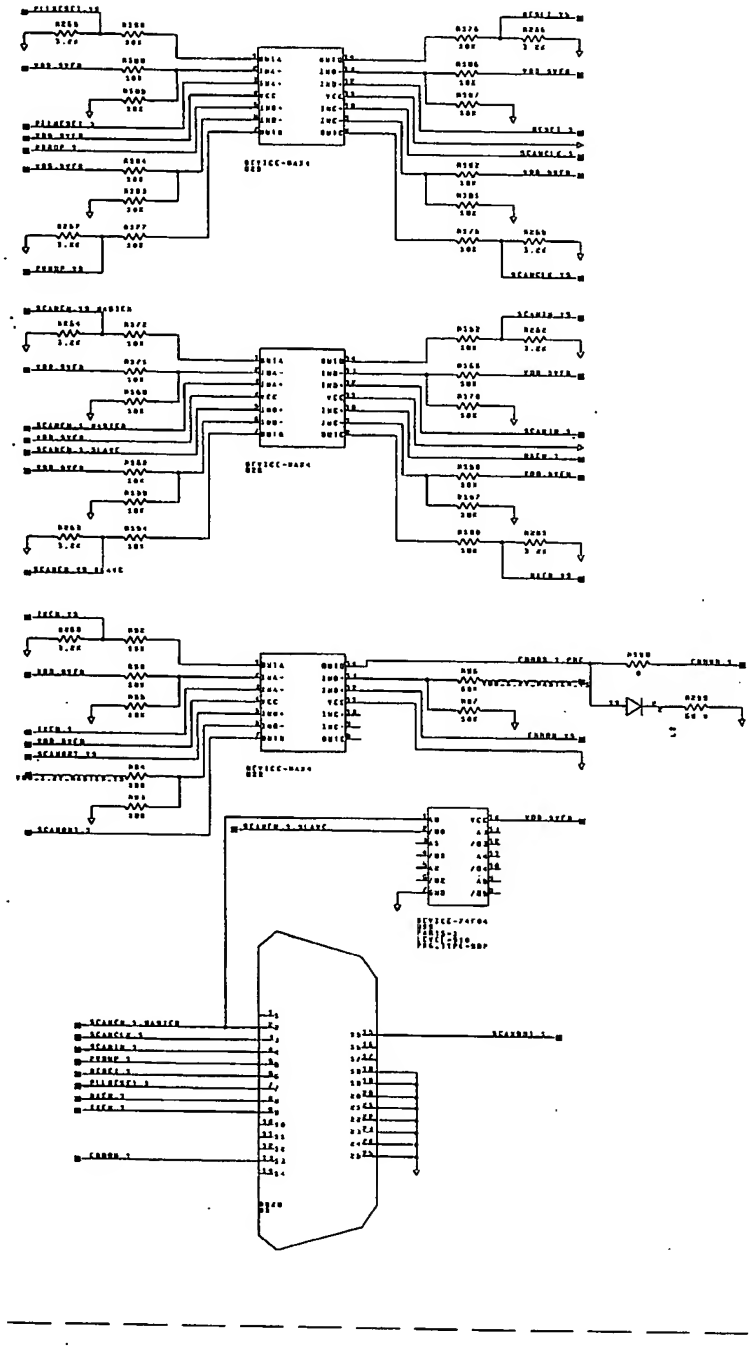


slave device specific

TD[0:7] connections

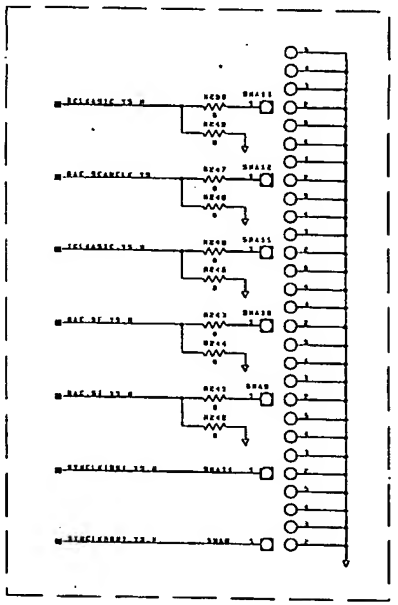


YS PC INTERFACE

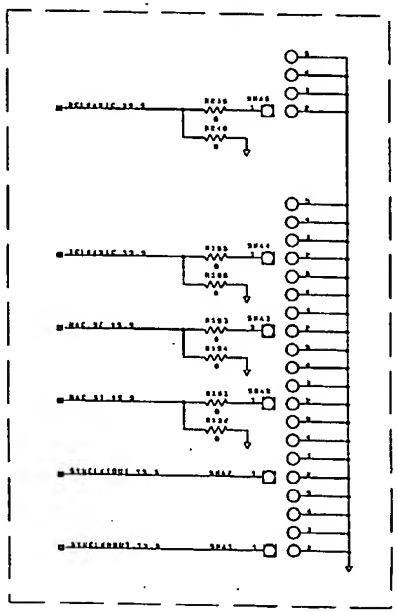


YS PC INTERFACE

lowspeed signals specific to the master device

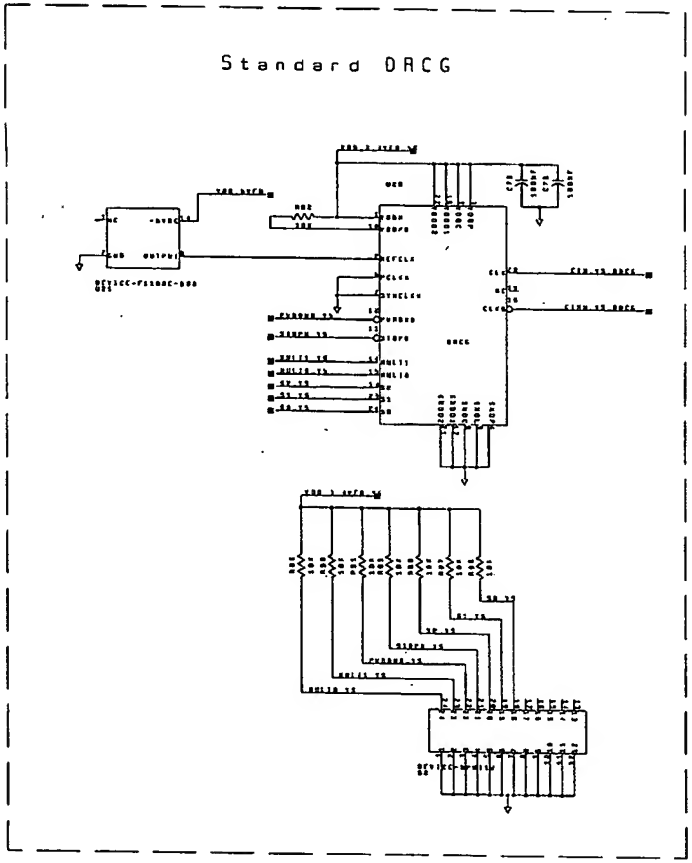


lowspeed signals specific to the slave device

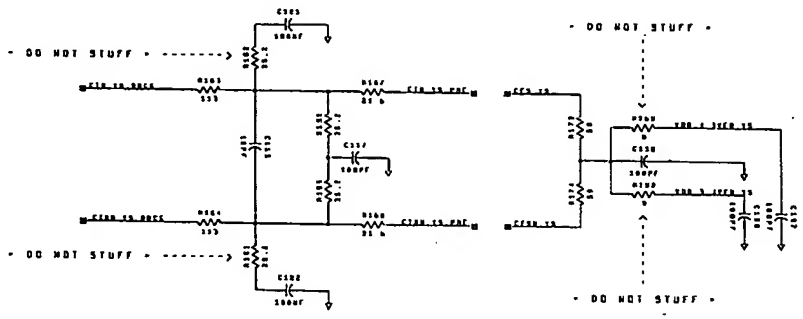


DRCG - YELLOWSTONE CONFIGURATION

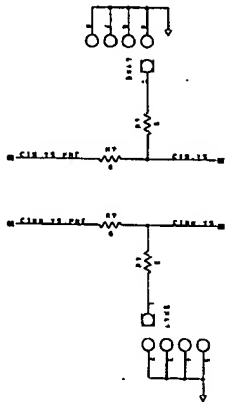
Standard DRCG

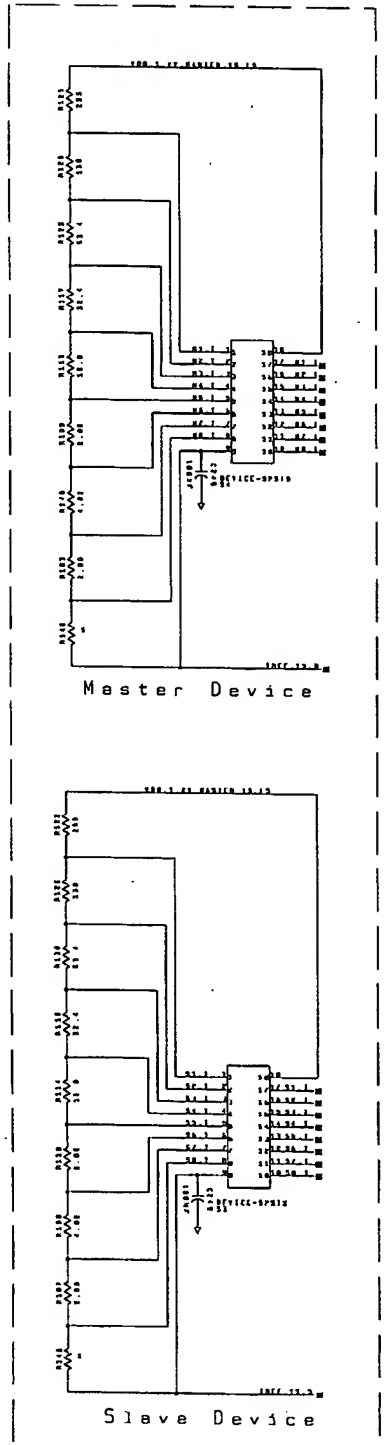


DRCG Termination - Yellowstone Configuration



DRCG SMA Option- Yellowstone Configuration



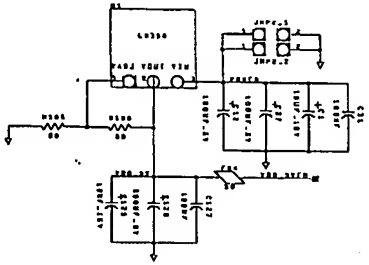


Mester Device

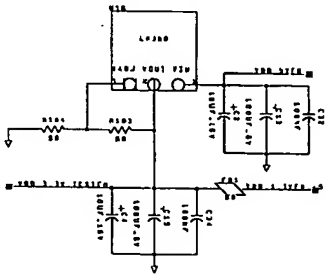
Slave Device

5V / 3.3V / 1.2V POWER SUPPLIES - YELLOWSTONE CONFIGURATION

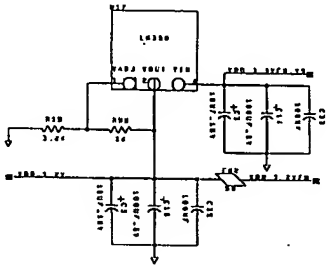
POWER - 5V Regulator



5V - 3.3V Regulator

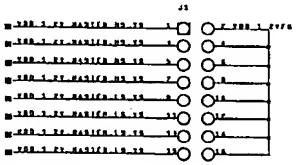


3.3V - 1.2V Regulator



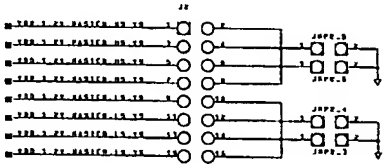
Major Plane Partition

(Master/Slave 1.2V Planes)

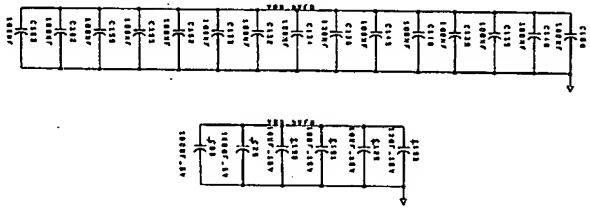


RB/LTCS Plane Partition

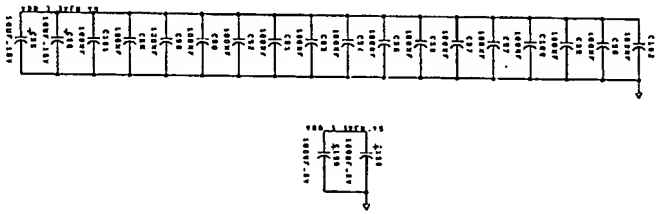
(Master/Slave 1.2V Planes)



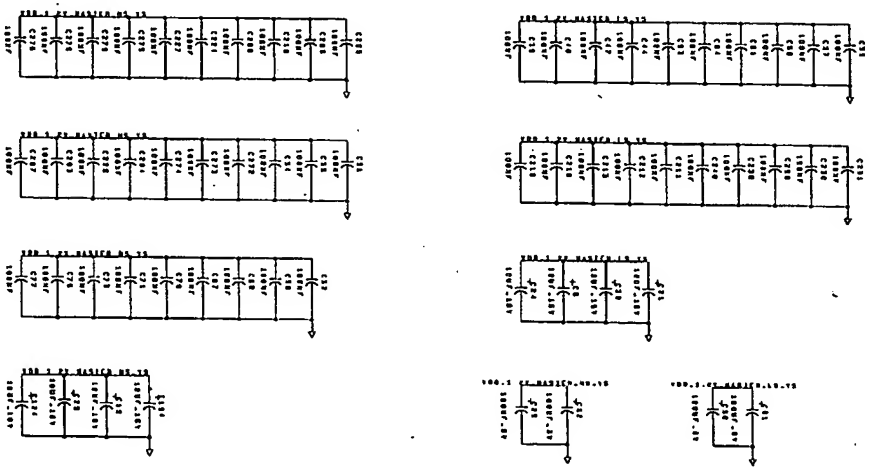
5V Plane (VDD_5VFB_YS) Bypassing - YS Section



DRCG (VDD_3.3VFB_YS) Bypassing - YS Section



YAC (VDD_1.2VFB_YS) Bypassing - YS Section

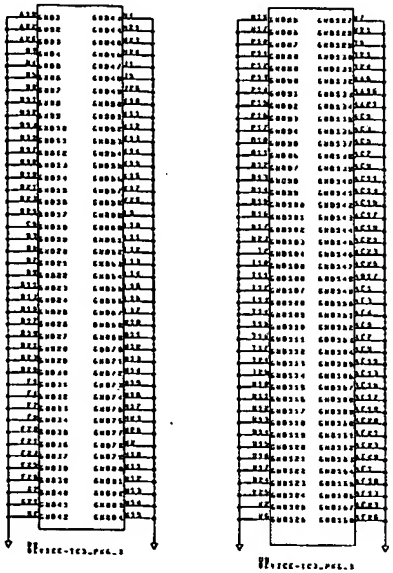


Master/Slave .

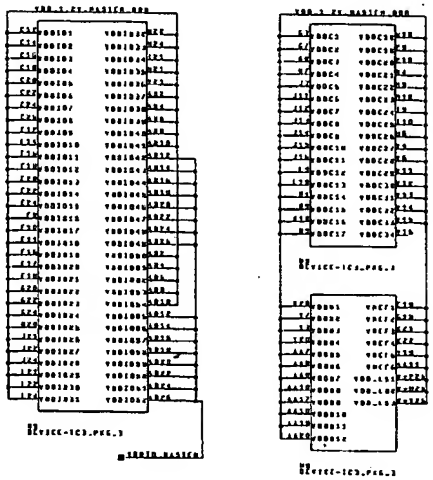
DDR Configuration

MASTER .

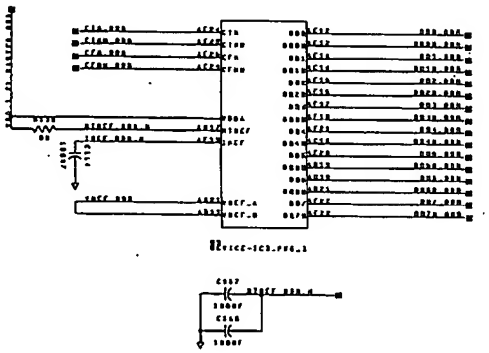
TC3 Package GND Pins



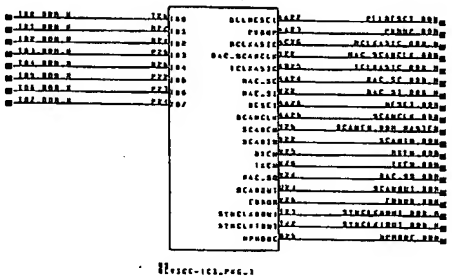
TC3 Package VDD Pins



TC3 Package HS Pins

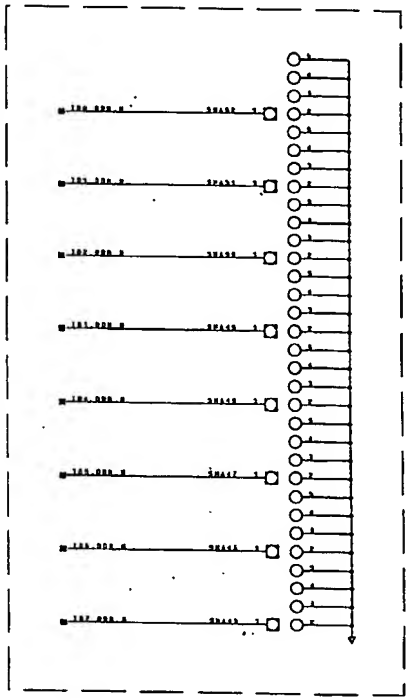


TC3 Package LS Pins



master device specific

TD[0:7] connections

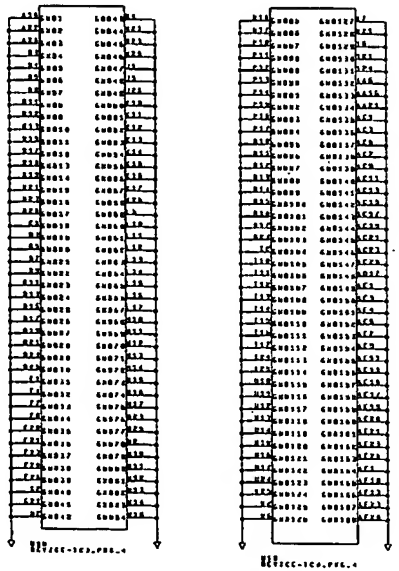


Master/Slave

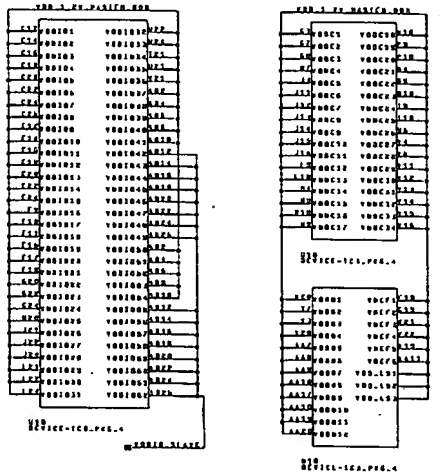
DDR Configuration

SLAVE

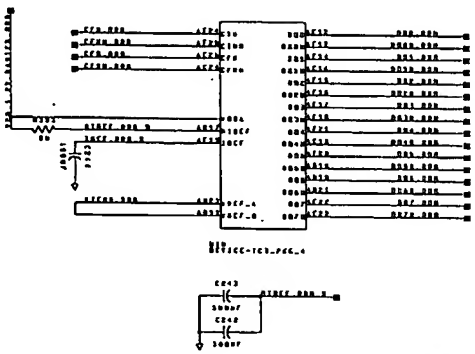
TC3 Package GND Pins



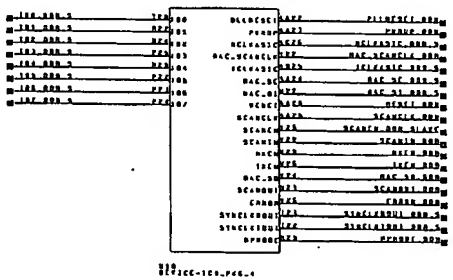
TC3 Package VDD Pins

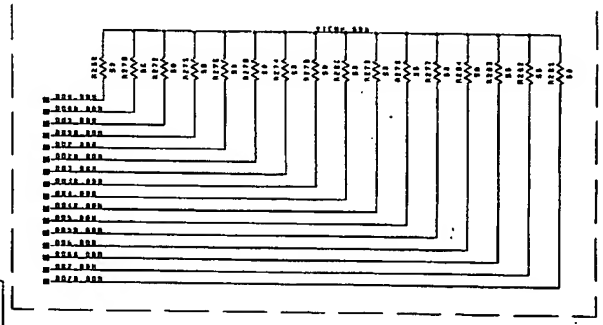


TC3 Package HS Pins



TC3 Package LS Pins

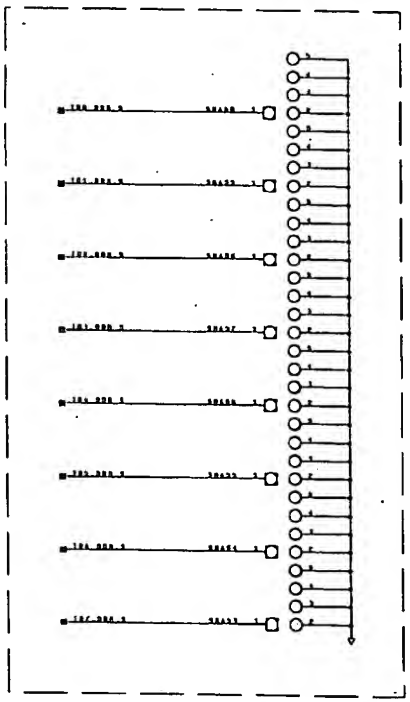




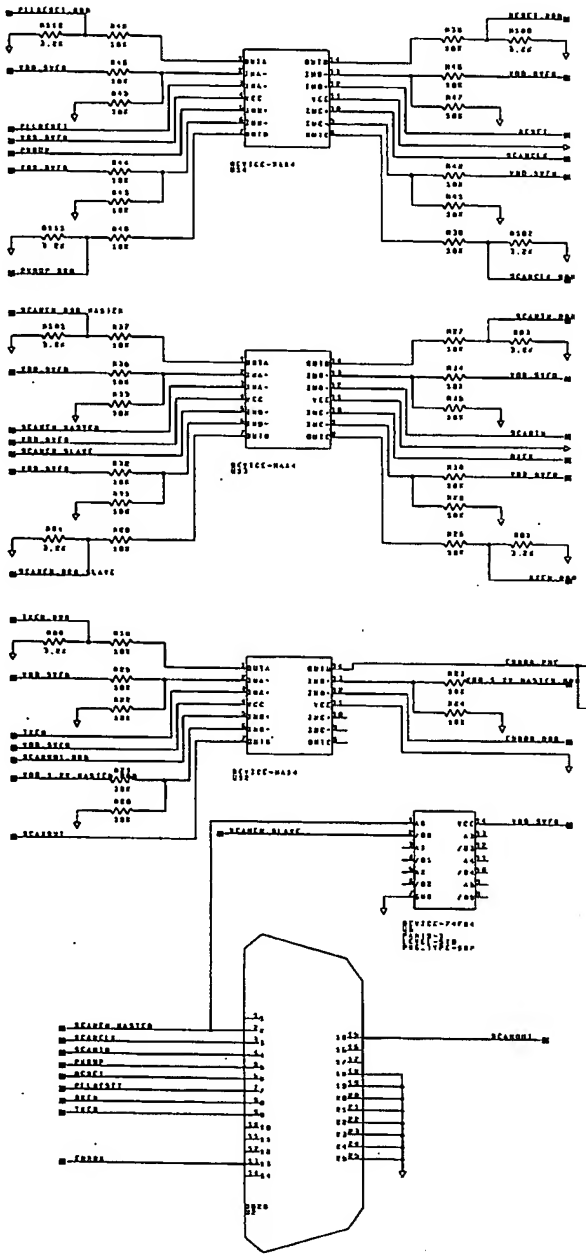
DDR Termination

slave device specific

TD[0:7] connections

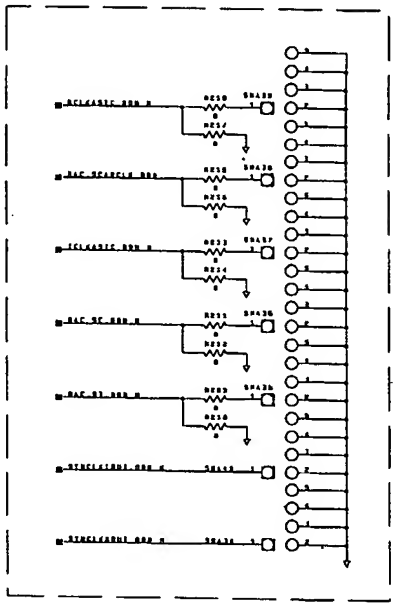


DDR PC INTERFACE

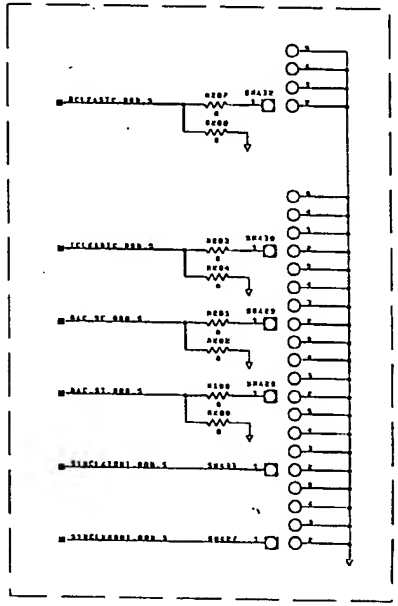


DDR PC INTERFACE

lowspeed signals specific
to the master device

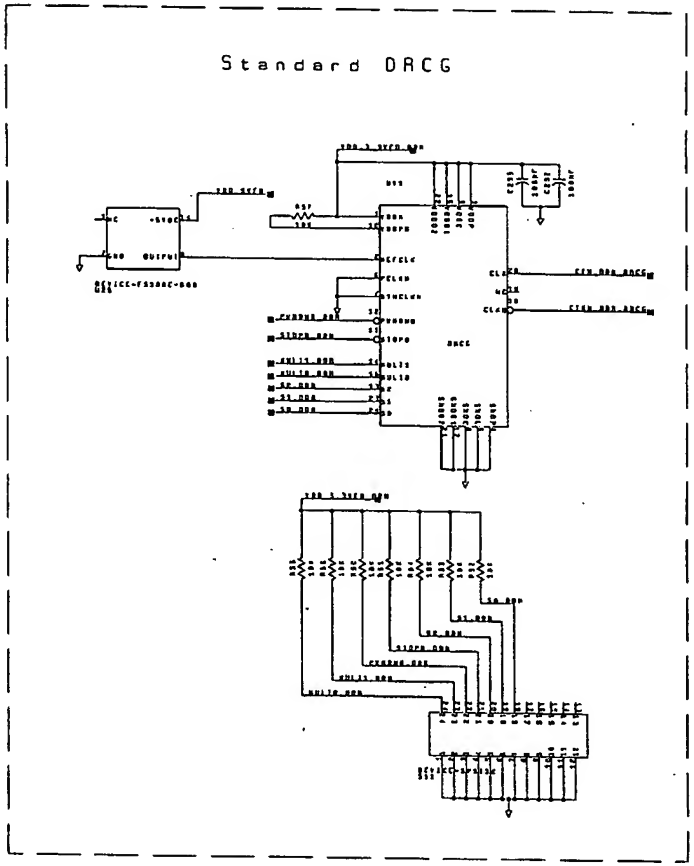


lowspeed signals specific
to the slave device

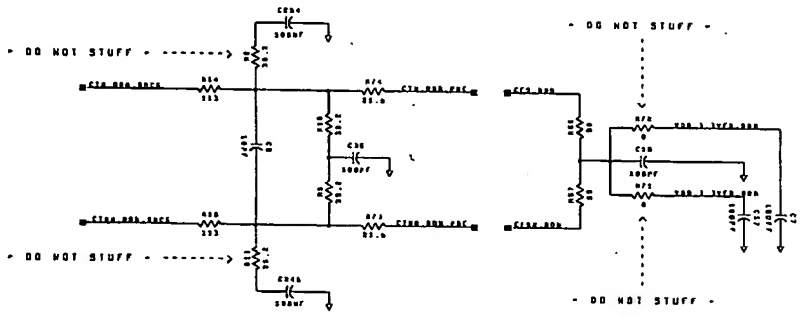


DRCG - DDR CONFIGURATION

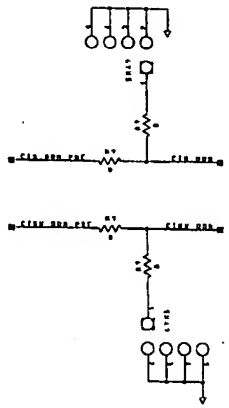
Standard DRCG

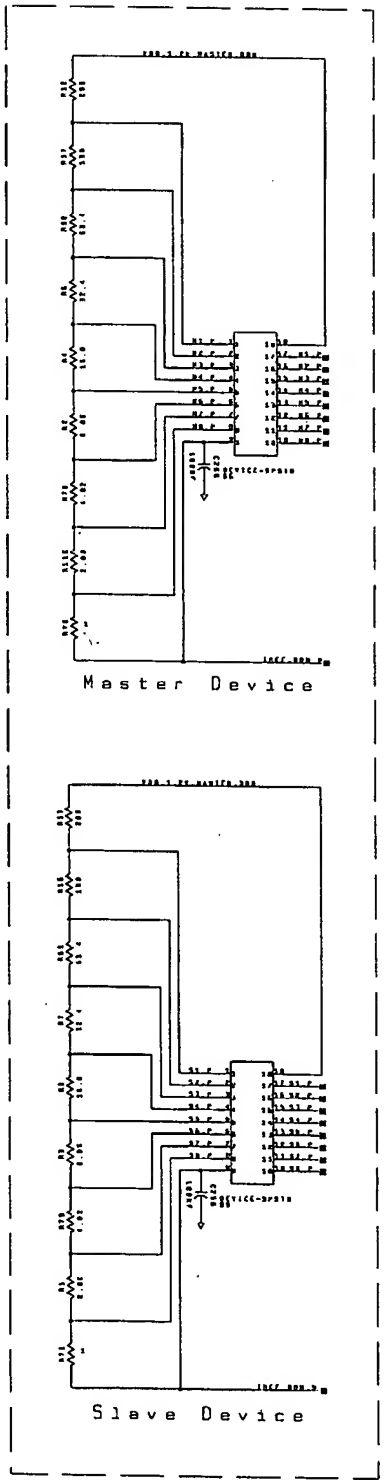


DRCG Termination - DDR Configuration



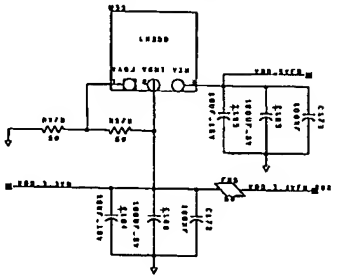
DRCG SMA Option- DDR Configuration



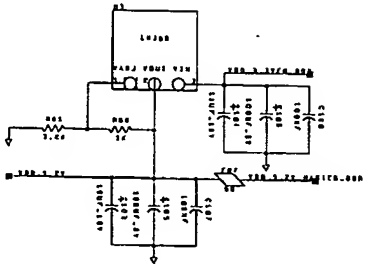

Master Device
Slave Device

5V / 3.3V / 1.2V POWER SUPPLIES - DDR CONFIGURATION

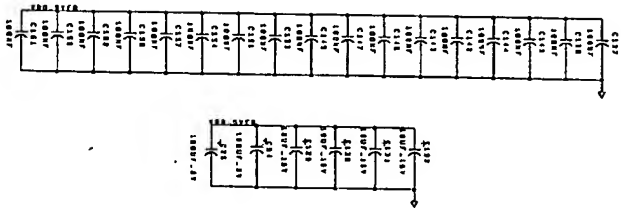
5V - 3.3V Regulator



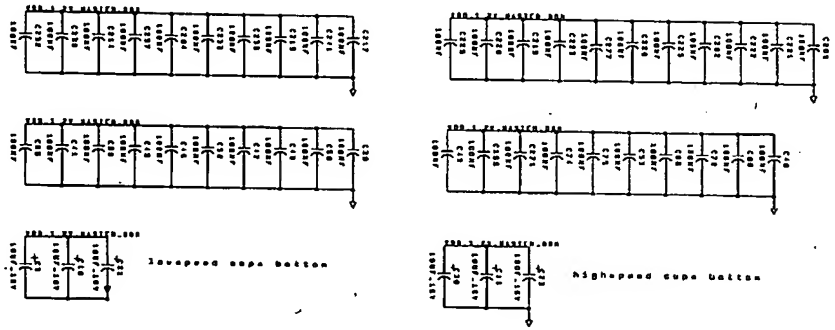
3.3V - 1.2V Regulator



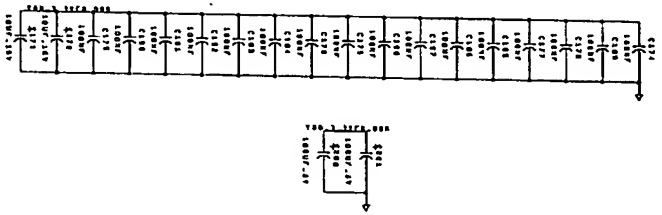
5V Plane (VDD_5VFB_YS) Bypassing - YS Section



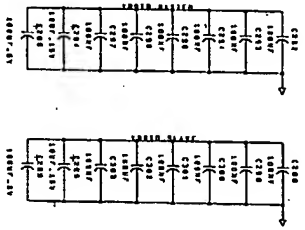
YAC (VDD_1.2VFB_YS) Bypassing - YS Section



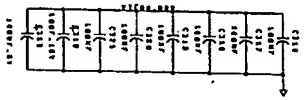
DRCG (VDD_3.3VFB_DDR) Bypassing - DDR Section



VDDIO Bypassing

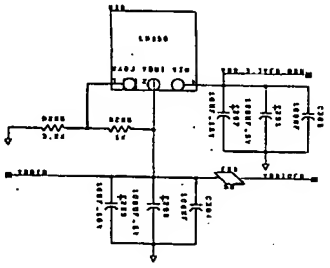


Vterm Bypassing



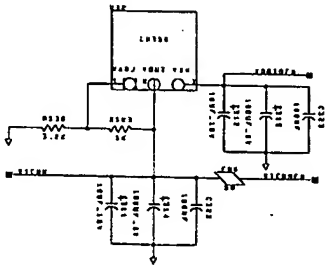
VDDIO Generation

3.3V - 2.5V Regulator



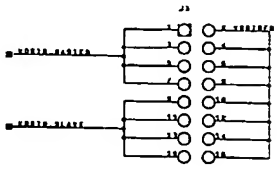
Vterm Generation

2.5V - 1.25V Regulator



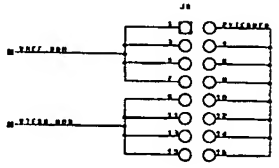
Major Plane Partition

(Master/Slave VDDIO Planes)



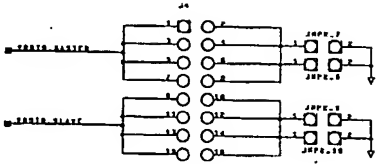
Major Plane Partition

(Master/Slave VDDIO Planes)



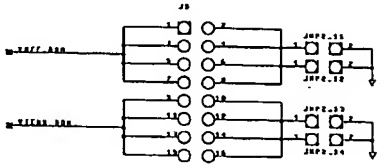
Plane Partition

(Master/Slave VDDIO Planes)



Plane Partition

(Master/Slave VDDIO Planes)



Wendy Goy

From: Yeung, Philip [pyeung@rambus.com]
Sent: Friday, July 26, 2002 5:53 PM
To: David Roelle; Dhat, Rob; Abhyankar, Abhijit
Subject: package and board release

Hello Rob/Dave,

TC3 is in reasonable shape. Let's not hold back on the package and board release.

package: 5 day fab, 5 day assembly
board: 10 day fab, 3/5 day assebmly

thanks

-- Philip

EXHIBIT F

For IP Group Use

RD-2106

Receipt Date: 7/18/02

Rev 1.5 4/19/2000

Rambus Invention Disclosure Form

Inventorship

Inventor Name: Scott Best _____ ext.

Residence Address: _____

Citizenship: _____ Division: ___

Inventor Name: Tim Chang _____ ext. _____

Residence Address: _____

Citizenship: _____ Division: _____

Inventor Name: Rich Perego _____ ext. _____

Residence Address: _____

Citizenship: _____ Division: _____

Inventor Name: _____ ext. _____

Residence Address: _____

Citizenship: _____ Division: _____

(If you believe that there are more than four inventors, please contact the IP group)

Potential Filing Deadlines

Invention in or to be incorporated in any Rambus product designs? No.

Name of product design: YAC and YDRAM _____

Date product design released or scheduled for release? _____

Invention disclosed or scheduled to be disclosed outside Rambus? ____

Nature of disclosure (e.g., customer meeting, white paper)? _____

Date of disclosure or scheduled disclosure? _____

Invention Disclosure

Title of Invention: Method and Apparatus for Testing and Characterization of High Speed Signaling Systems _____

Use the following outline to describe your invention, preferably within two or three pages. Include/attach any diagrams or other documents helpful to understanding the invention.

1. Problem addressed by the invention

In digital systems which utilize high speed signaling, there is a problem with both characterizing and testing the receive circuit and transmit circuit on each component. The problem is twofold.

[1] High speed circuitry requires high speed test equipment. The cost of the equipment increases with the signaling rate of the circuitry under test. This means that high speed testing will be more costly. It is also possible that high speed test equipment is not available at all semiconductor manufacturers. This could limit the number of manufacturing sources for the components of a high speed system.

[2] High speed circuitry is sensitive to its environment. Characterization and testing of a component in isolation may give non-optimal results if the test environment does not reproduce the system environment closely enough. This can require additional testing margin be added to the range limits of the specification parameters of the component. Characterization and testing of a component in its system environment can also give non-optimal results because of the loading effects of the signal connections to the test equipment. Again, this can result in the need to expand parameter ranges to accommodate testing margins.

EXHIBIT G

2. Description of the invention and how it overcomes/mitigates the problem

There are typically a number of voltage, current, and timing parameters which specify the operating conditions under which the receive circuit and transmit circuit are evaluated. There are also a number of voltage, current, and timing parameters which specify the operating characteristics which the receive circuit and transmit circuit must satisfy.

Characterization is the process of determining how much margin exists in each of the parameters in order to set the appropriate minimum and maximum limits. Testing is the process of ensuring that each parameter falls within the allowable limits for a particular component. Both characterization and testing can be conducted at the wafer level (probing the component before packaging), at the package level, and at the system level. Testing and characterization at the system level can be conducted at initialization time, in between periods of normal system operation, and after a failure is detected during system operation.

There are a number of features possessed by the receive circuit and transmit circuit of the YAC interface for controller components. These include the following:

[1] Sample point of the receive circuit continuously adjustable (by programmable register value) over a range of many bit times.

[2] Drive point of the transmit circuit continuously adjustable (by programmable register value) over a range of many bit times.

[3] Reference voltage for input comparator of the receive circuit continuously adjustable (by programmable register value) over a range.

[4] Sink current of the transmit circuit continuously adjustable (by programmable register value) over a range.

[5] Resistance of the termination circuit continuously adjustable (by programmable register value) over a range.

By connecting pairs of component pins together during component testing at the wafer level and package level, virtually all of the specification parameters can be tested. Further, by appropriately programming the various registers listed above, the operating conditions can be varied, allowing the amount of margin to be characterized.

The YDRAM has a subset of the features listed above. Nonetheless, by pairing two YDRAMs, or by pairing a YDRAM with a YAC on a custom test chip, the same component testing at the wafer level and package level is possible, permitting virtually all of the specification parameters to be tested.

In a system, the YAC and YDRAM components can test one another, using a similar testing procedure.

3. Advantages of the invention over prior techniques

The principle advantage is that the cost of a high speed test system are avoided by using component-to-component testing. This reduces product cost, and increases the number of potential manufacturing sites.

By doing all testing and characterization with one component testing another, or testing itself, the testing procedure at the wafer, package, and system level will be very similar. This will help limit the amount of test margin needed, and will permit much of the testing software to be shared.

4. Value of the invention to Rambus

This test and characterization alternative is important to a fabless company like Rambus.

Records of Invention

Serial nos. and page nos. of notebooks or other records containing notes and date of invention:_____

Are there any non-documentary items useful to establish conception of the invention or reduction of the invention to practice? (e.g., models, prototypes, etc.) _____ If yes, please explain: _____

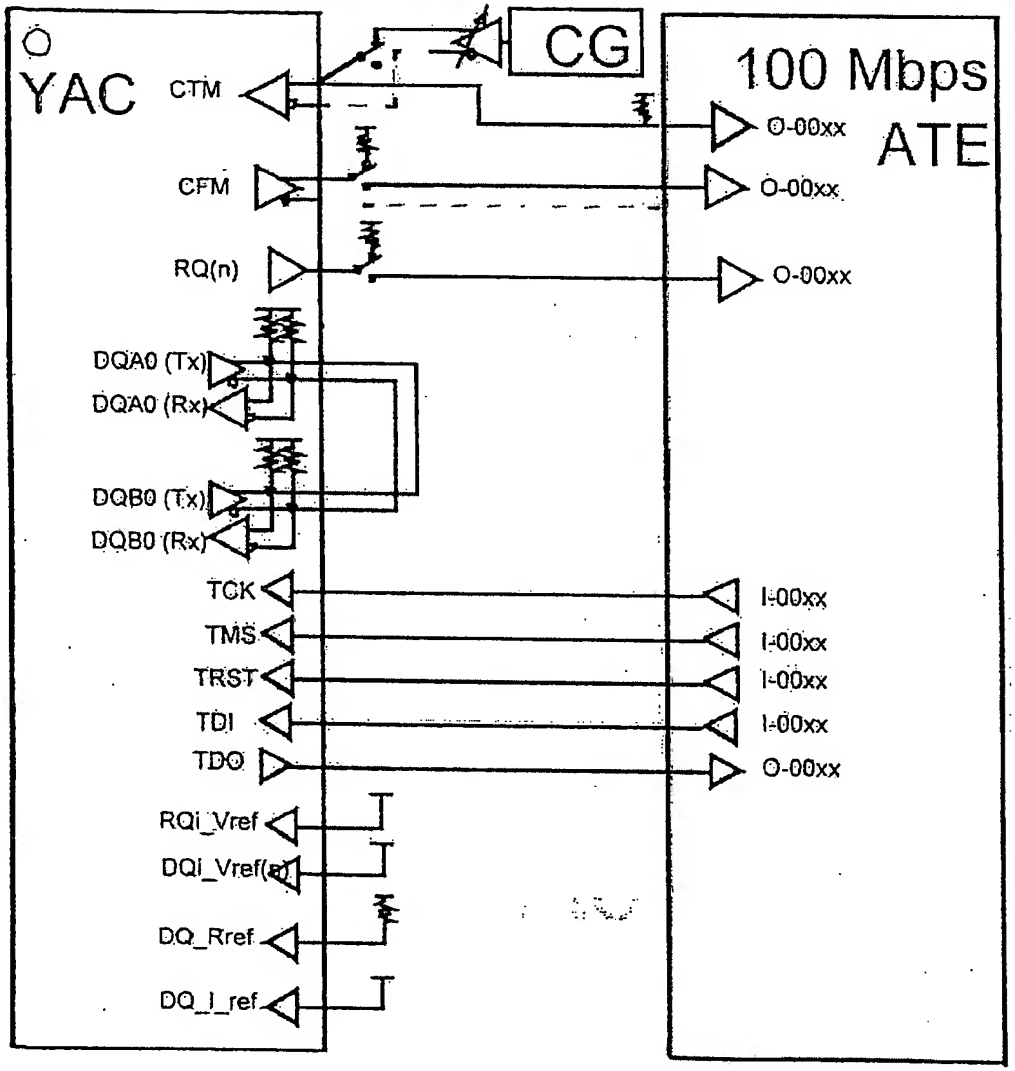
ATTACH COPIES OF ANY DOCUMENTS USEFUL TO ESTABLISH DATE OF INVENTION (e.g., invention notebook pages, email prints, test/simulation results, draft specifications, etc.)

Name of individual submitting disclosure (please print): Frederick A. Ware

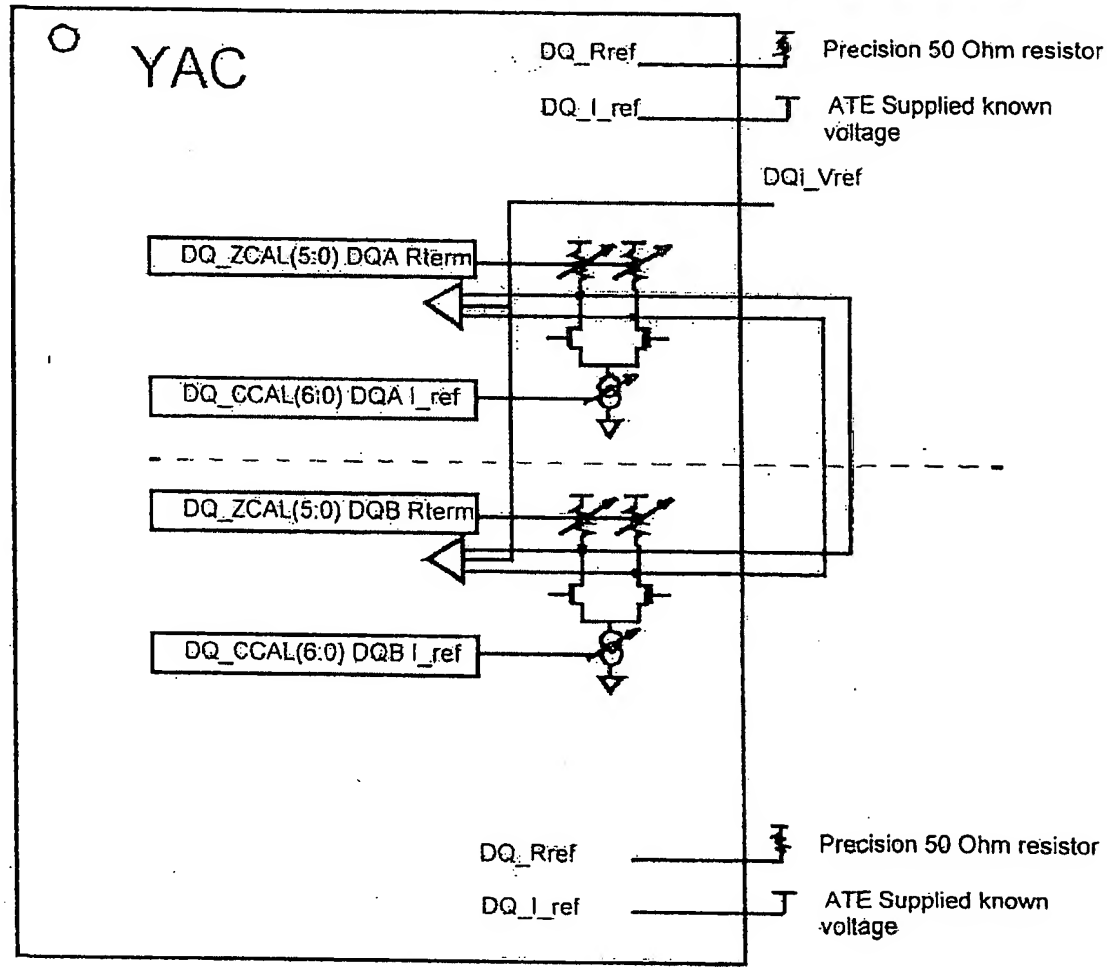
Signature: _____ Date: 07/18/02

Witness Signature: _____ Date: 07/18/02

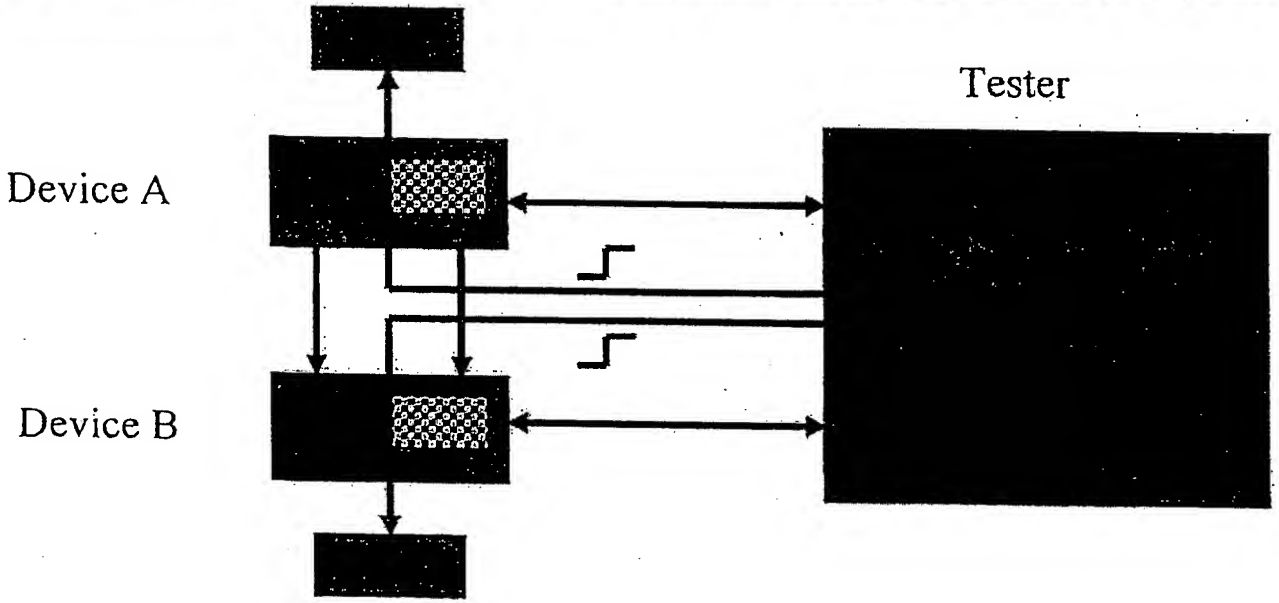
YAC Connection to 100Mhz ATE



DQ Loopback Config & Resources

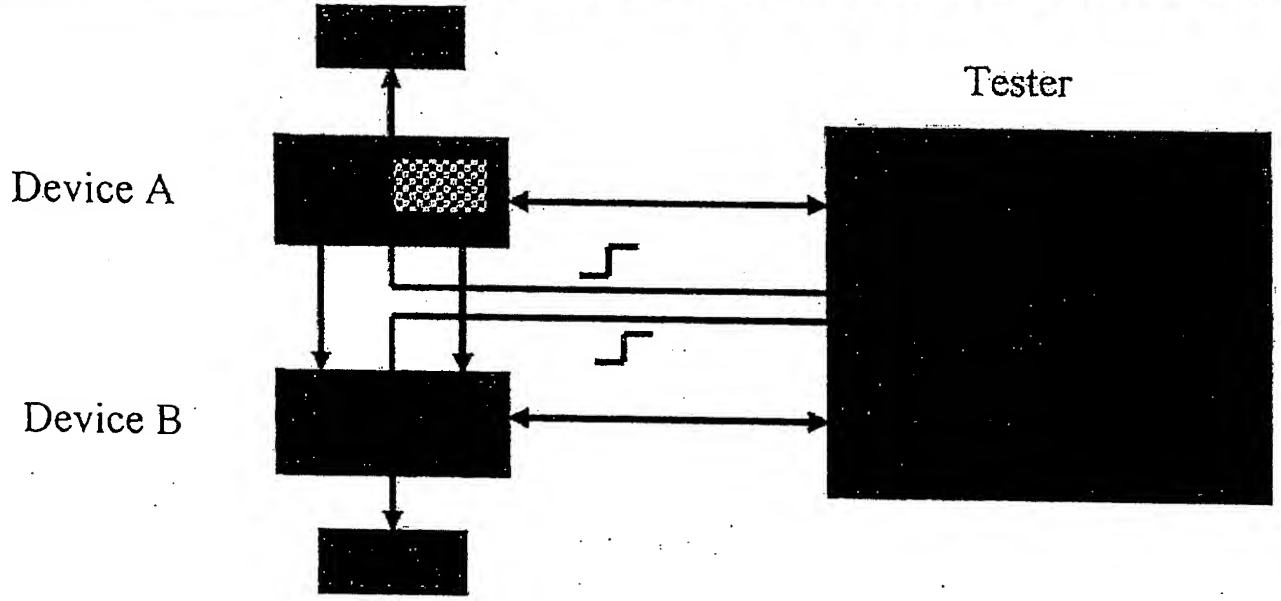


YDRAM DST Example



- 1. Load test patterns to Device A via Serial I/F & RQA
  - Scan pattern into WB…send COL packet to perform write to core
- 2. Set initial phase of CFM_B & RQ_B
- 3. Read patterns from Device A while writing to Device B
- 4. Read patterns from Device B & scan out on Serial I/F B

YDRAM DST Example



- 5. Read patterns from Device B & write to Device A
- 6. Read patterns from Device A & scan out on Serial I/F A
- 7. Adjust phase of CFM_B and RQB…allow PLL to lock
- 8. Repeat at Step 3. Sweep through 1 bit time (312 ps)
  - ~64 phase steps on CFM

BBC

From: Barbara Courtney [bcourtney@sgcpatentlaw.com]
Sent: Wednesday, October 02, 2002 3:35 PM
To: 'ware@rambus.com'; 'Paulal@rambus.com'
Cc: 'amullany@rambus.com'
Subject: Draft RA280

HI All,

Attached are text and figures for the draft. Thanks for your help so far and thanks in advance for the review. The figures include some titles that will not be in the final version, but it they might be helpful for your review because the figures have been reordered. Contact me anytime to discuss.

Regards,
Barbara

EXHIBIT H